UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/444,173	11/19/1999	FONG PONG	HP10981470-1	8306

7590 03/17/2003

IP ADMINISTRATION
LEGAL DEPARTMENT 20BN
HEWLETT PACKARD COMPANY
P O BOX 10301
PALO ALTO, CA 943030890

EXAMINER	
SONG, JASMINE	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 03/17/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/444,173	Applicant(s) PONG, FONG	
	Examiner Jasmine Song	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Detailed Action

Specification

1. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 6 recites the limitation "the requested block of data" in lines 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said

subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Doren et al., U.S. Patent 6209,065 B1.

Regarding claims 1, 9 and 19, Van Doren et al. teach a multiprocessor system comprising:

two or more processors(Fig.1, element 102-108), each in communication with a shared memory (Fig.1, element 150) via a memory controller(Fig.1, element 200);

the processors in communication with the memory controller for issuing a request for data (col.6, lines 57-60 and 66-67 or col.8, lines 67 to col.9, lines 2), each of the processors and the shared memory being capable of storing a copy of the requested data (col.6 lines 1-14 and lines 20-25), and each copy of the requested data being associated with state indicating whether the copy is valid or invalid (col.6, lines 31-39 and col.7, lines 53-57).

each of the processors and the shared memory being responsive to a request to check itself for a valid copy of a requested data (col.7, lines 3-21) and response to the request (col.7, lines 22-24; col.8, lines 47-50 and col.9, lines 28-32).

Van Doren does not **specifically** teach that **only** one processor or the shared memory having the valid copy responds to the request. However, it is well known in the memory art of multiprocessor systems for the ownership of the requested data be a necessary component in which element provides the valid data to the requesting device In order to maintain coherency of data within these systems only one processor will have the ownership rights for the data and depending on other activities in the system,

the data may be in a modified state and either written back to the main/shared memory or held by that processor in a memory (cache, buffer or other type memory) until it is time to perform the write-back operation to update the main/shared memory. In this situation, the valid data can only be provided by the processor that owned the data in a state that allowed the data to be modified or by the main/shared memory if the modified data has been written back to the main/shared memory. It would have been obvious to one of ordinary skill in the memory art at the time the invention was made for the valid data to be provided to the requester by either the processor that modified the data or the main/shared memory because the processor that modified the data or the main/shared memory are the only sources for the valid data and official notice is taken thereof. Maintaining coherency in a multiprocessor system with a main/shared memory requires specific maintenance of the ownership of the data, otherwise, the data becomes corrupt and the data within this system is no longer reliable. Combining the requirement of only one processor having ownership rights to modify the data which sets forth situations in which only the processor with such ownership rights and possibly the main/shared memory also contain the modified data with the other limitations of the claims provides a well known method for maintaining data coherency within the system.

Regarding claims 2 and 10, Van Doren teach each of the processors (Fig.1, element 102-108) communicates with the memory (Fig.1, element 150) via a memory controller (Fig.1, element 200) and each of the processors has a point-to-point link

(Fig.2) with the memory controller for issuing a request for a block of data (Fig.1, col. 5, lines 39-42 and Fig.2, col.7, lines 48-50) to the memory controller (Fig.1, element 200).

Regarding claims 3 and 11, Van Doren teach each point-to-point link includes two dedicated and unidirectional links (Fig.2, col.7, lines 31-35).

Regarding claims 4 and 12, Van Doren teach the point-to-point links are control links for sending and receiving requests for blocks of data (Fig. 2, col.7, lines 35-39).

Regarding claims 5 and 13, Van Doren teach each of the processors has a control path point-to-point link for sending and receiving requests for blocks of data (Fig. 2, col.7, lines 35-39), and a data path point-to-point link for sending and receiving blocks of data (Fig. 2, four data paths connected between shared memory and processors).

Regarding claim 6, Van Doren teach the processors and shared memory that have an invalid copy of the requested block of data drop the request without responding (col.7, lines 15-18).

Regarding claim 7, Van Doren teach tracking an identification of a processor that currently has a data block (col.6,lines 20-23); and in response to a cache miss in a requesting processor, using the identification to specifically target a read request to the processor that currently has the requested data block (col.6, lines 57 to col.7, lines 7).

Regarding claim 8, Van Doren teach maintaining a directory indicating the one or more processors that have a copy of a block of data (Fig.1, element 160); when the block of data is modified, using the directory to issue a write invalidation or write update only to the processors that have the copy of the block of data (col.6, lines 15-20).

Regarding claims 14,15 and 16, Van Doren teach a directory indicating which processors have a copy of a data block (Fig.1, element 160); wherein the processors are in communication with the directory to identify which other processors have a copy of the data block, and directing requests for the data block only to processors that have a copy of the data block (col.6, lines 20-25 and col.6, lines 66 to col.7, lines 21).

Regarding claim 17, Van Doren teach the memory controller (Fig.2, element 200) is in communication with a shared cache (Fig.2, element 160), separate from caches of the processors (Fig.1), for buffering most frequently accessed data block (col.6, lines 31-41).

Regarding claims 18, Van Doren teach each block has state information indicating which processor currently has a valid copy of a data block, and wherein the processors utilize the state information to specially address a processor having the valid copy in response to a cache miss in a requesting processor (col.6, lines 20-25).

Regarding claim 20, Van Doren teach each of the processors and the shared memory is in communication with a control path interconnect (Fig.1 and Fig.2, the four arrows between shared memory and four processors), and each of the processors is in communication with the control path interconnect via a point-to point link for receiving and sending requests for blocks of data (Fig.1 and Fig.2; col.7, lines 31-42);

each of the processors having a corresponding request queue connecting the point-to-point link of the processor to the control path interconnect (Fig.2), and each of the processors having a corresponding snoop queue (Fig.2, element 222-230) connecting the point-to-point link of the processor to the control path interconnect (Fig.2, col.7, lines 31-42);

the request queue (Fig.2, element 212-220) in communication with a corresponding processor for buffering requests for blocks of data by the processor and issuing the requests to other processors via the control path interconnect (col.7, lines 31-42); and

the snoop queue (Fig.2, element 222-230) in communication with a corresponding processor for buffering requests for blocks of data destined for the processor (col.7, lines 31-42).

Regarding claims 21 and 22-23, Van Doren teaches that the processor or the shared memory responding to the request is configured to respond to the request asynchronously. This limitation is taught as the processor or the shared memory responding to the request is out of order (col.5, lines 63-67 and col.7, lines 63-65).

Response to Amendment

6. Applicant's arguments with respect to claims 1-20 filed on 11/12/2002 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

VanDoren et al., U.S. Patent 6279084 B1 teaches that shadow commands to optimize sequencing of requests in a switch-based multi-processor system.

Laudon et al., U.S. Patent 6182195 B1 teaches that a system and method for maintaining coherency of virtual-to-physical memory translations in a multiprocessor computer.

McDonald et al., U.S. Patent 6012127 teaches that a multiprocessor computing apparatus with optional coherency directory.

Liberty., U.S. Patent 6275900 B1 teaches that a hybrid NUMA/S-COMA system and method.

8. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

9. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do H. Yoo can be reached on 703-308-4908. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

March 10, 2003

Kevin L. Ellis
Primary Examiner

****

IMPORTANT NOTICE

The Examiner's art unit number has changed from 2187 to 2188 due to the recent realignment of workgroup 2180. Please use art unit 2188 on all correspondence related to this case.

****